REMARKS:

Claims 1-19 were presented for examination and were pending in this application. In an Official Action dated October 5th, 2005, claims 1-11 were rejected and claims 12-19 were subject to a restriction requirement. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below. A summary of the Examiner Interview that took place on December 15th, 2005 is incorporated into the following remarks.

Applicants herein amend claims 1, 6, and 9. Claims 12-19 are cancelled without prejudice or disclaimer. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Rejection Under 35 USC § 112, Paragraph 2

In the 5th paragraph of the Office Action, Examiner has rejected claims 1-4, 5, 6, 9, and 10 as allegedly not specifically pointing out and distinctly claiming the subject matter that the Applicant regards as the invention.

Claim 1 was rejected for allegedly having insufficient antecedent basis for the limitations "the first control status register" in lines 27 and 28 and "the second control status register" in lines 29 and 30. Claim 1 has been amended to clarify the antecedent basis for these claims elements.

Claim 6 was rejected for allegedly having insufficient antecedent basis for the limitation "the context" in lines 2-4. Claim 6 has been amended to clarify the antecedent basis for this claim element and for the element "source data register".

Claim 9 was rejected for allegedly having insufficient antecedent basis for the limitation "the context" in line. Claim 9 has been amended to clarify the antecedent basis for this claim element.

Claims 1, 6, and 9 have been amended to clarify the antecedent basis for various claim elements. This amendment of the claims is made so as to more clearly define the invention, and not to narrow their scope of protection with respect to the prior art, or with respect to potentially infringing devices/compositions/articles.

Claims 2-4 were rejected for incorporating the defects of Claim 1, and Claim 10 was rejected for incorporating the defects of claim 9. As Claim 1 and Claim 9 have been amended to clarify the antecedent basis for various elements, Claims 2-4 and 10 incorporate the clarified language and are no longer defective. Applicants submit that claims 1-4, 5, 6, 9,

and 10 are in condition for allowance and request that the rejection under 35 USC 112 be withdrawn.

Response to Rejection Under 35 USC 102(e)

In the 13th paragraph of the Office Action, Examiner rejects claims 1-11 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,542,991 to Joy et al. ("Joy"). This rejection is now traversed.

Claim 1 recites:

> a first set of data storage devices capable of storing a first state of said embedded processor, wherein said first state is the state of the embedded processor during the execution of the first program thread;
> a second set of data storage devices capable of storing a second state of said embedded processor, wherein said second state is the state of the embedded processor during the execution of the second program thread;
> wherein at least said first set of data storage devices includes a first control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is not included in the first set of data storage devices;

The invention beneficially allows a first thread to access and store information into the state of a different thread. For example, when executing an instruction from a first context one or more of the source or destination registers can be from a set of registers not associated with the first context.

In contrast, Joy teaches a system for rapidly switching between contexts. In the system taught by Joy, an instruction of a first context cannot use either source or destination registers outside of that first context. To facilitate fast switching, registers are organized in a multi-dimensional register file. "The concept of a multi-dimensional register file applies to the support of context switching so that the individual planes 1310 represent a separate

context. Context switching between microtasks is rapidly accomplished by simply changing the context number, as shown in Fig. 13 as changing the window pointer 1312." (Col. 27, ln. 21-25)

The current window decode in Joy determines which context will be executed and which associated set of registers (which plane in the multi-dimensional register file) will be accessible. The context is switched by changing the current window pointer. Therefore, the currently executed instruction only has access to the memory locations associated with its own window pointer. (Throughout this response, reference is made to a "currently executed instruction". Applicants understand that multiple instructions may be present in a pipeline concurrently. The case of a single-instruction pipeline will be discussed herein for the purposes of simplicity.)

Joy elaborates on the operation of a multidimensional register file with reference Fig. 16. Fig. 16 is a schematic diagram illustrating a bit storage circuit for a multidimensional register file. An assembled copy of Figs. 16(a) and 16(b) is provided for the reference of the Examiner:

FIG. 16A

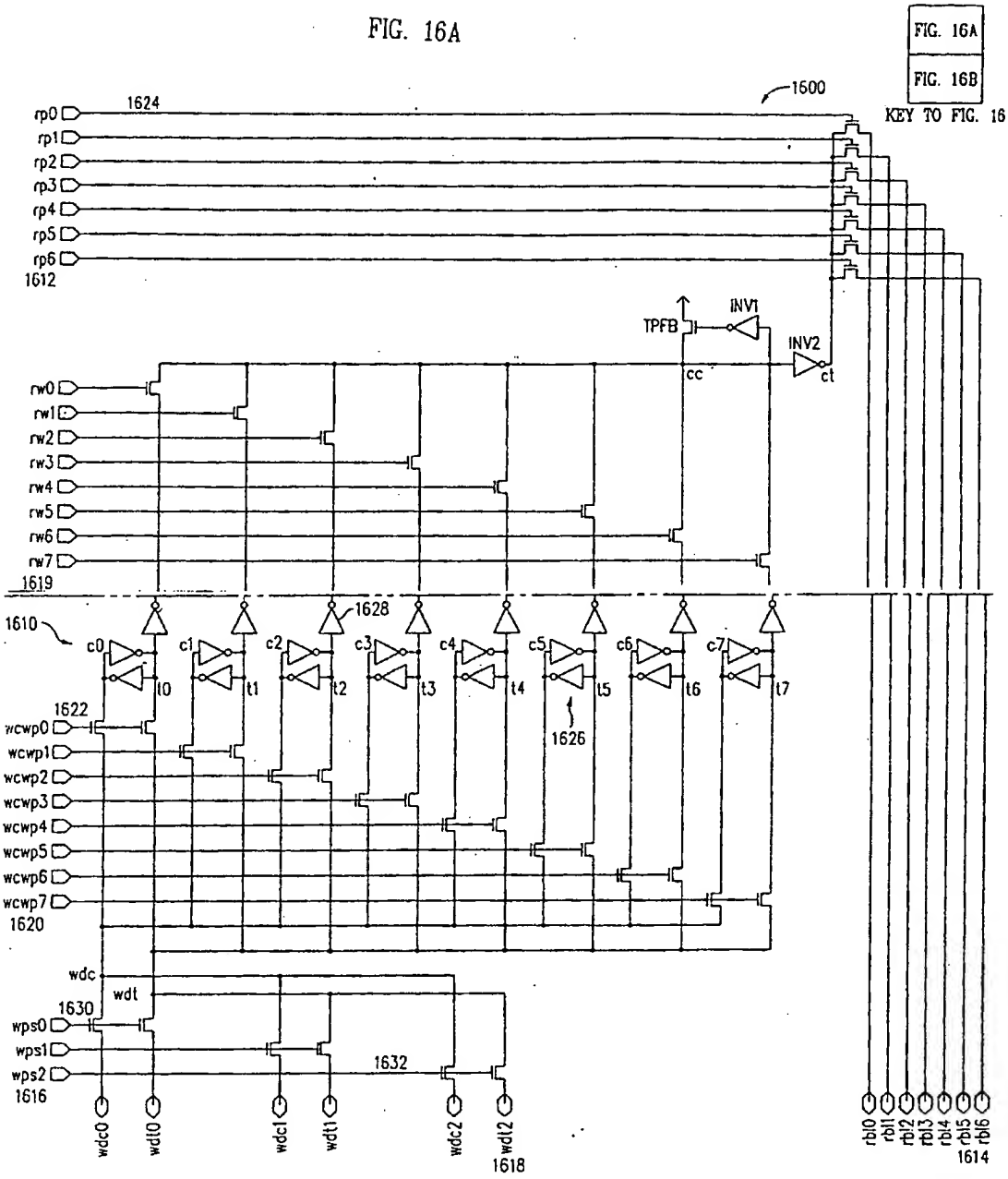

FIG. 16B

Fig. 16 illustrates a single lateral register location at a plurality of depths ("one bit of the local registers for the multidimensional register file", col. 28, ln. 45-46). Eight storage cells 1610, c0-c7, are capable of independently storing 8 bits. Each cell 1610 is associated with exactly one window, and is readable or writable only when that window is asserted.

For example, assume that a window is asserted for the purposes of writing. Exactly one write window 1620 (one of the control lines labeled 'wcwp' in Fig. 16) will be asserted. "The storage cell 1610 does not allow multiple write operations to the same register at one time." (col. 28, ln. 55-57) The write window 1620 is asserted by the "current window pointer 1622". (col. 28, ln. 55; Fig. 16) The depth in the multidimensional register file corresponds to the *current* window, that is, it is determined by the context of the currently executed instruction. In the multidimensional register file of Fig. 16, the assertion of a window provides access to exactly one bit cell—the bit cell corresponding to the current context window. For example, suppose the context of the currently executed instruction is window 0. The write window pointer 1622 will select wcwp0. Assertion of wcwp0 will open the gates to the right of the reference figure 1622 and allow writing to the bit cell c0/t0 associated with window 0 through the write ports 1616. Thus, in contrast to independent claim 1, in the multidimensional register file disclosed by Joy the instructions of a first context only have the capability of reading or writing from their same context.

In Figs. 17-18, Joy teaches sharing of registers between adjacent windows in a multidimensional register file. Fig. 18 is a schematic diagram illustrating a bit storage circuit for a multidimensional register file. An assembled and annotated copy of Figs. 18(a)-18(d) is provided for the reference of the Examiner:

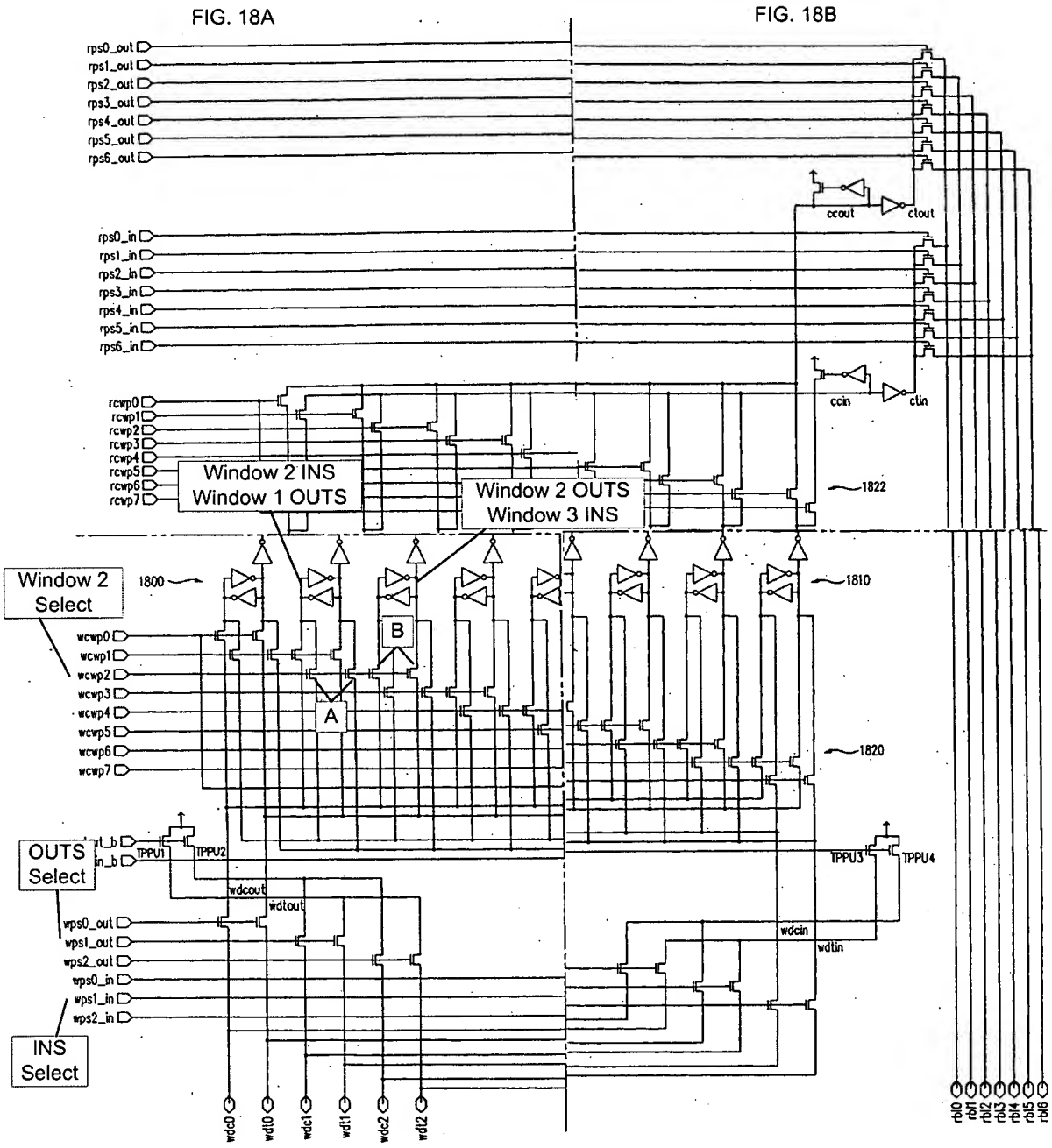

FIG. 18C

FIG. 18D

Fig. 18 illustrates a single lateral register location at a plurality of depths. As in Fig. 16, eight storage cells 1810 are capable of independently storing 8 bits. In contrast to Fig.

16, however, registers are shared among adjacent windows, and each cell 1810 is associated with exactly two windows. A given cell 1810 is readable or writable only when one of the two windows with which it is associated is asserted. (Fig. 18; col. 30, ln. 15-20) As in Fig. 16, exactly one write window pointer is asserted, the window pointer corresponding to the window of the currently executed instruction.

For example, assume that the context of the currently executed instruction is window 2. The control line wcwp2 will be asserted. Assertion of wcwp2 will open the gates labeled A and B and allow writing to either the bit cell labeled Window 2 INS or the bit cell labeled Window 2 OUTS. Writing of the INS or the OUTS is determined by the control lines wps*_out and wps*_in of the bottom left corner of the figure. For example, if wps0_out is asserted in combination with wcwp2, the OUTS of window 2 will be available for writing. Thus instructions of a first context have the capability of reading or writing from either the INS or the OUTS of their same context. However, Joy does *not* disclose instructions of a first context reading or writing outside of the bit cells associated with that context.

The system of overlapping registers taught in Figs. 17-18 allows a first context to pass parameters to a second context by the sharing of bit cells. The INS of one context are the same physical location in memory as the OUTS of another context. For example, suppose an instruction of window 2 writes some data to its OUTS registers. As illustrated in Fig. 18 and explained above, this data will be stored in the bit cell labeled window 2 OUTS. An instruction of window 3 will then have access to that data because the OUTS of window 2 *are the same location in memory* as the INS of window 3. (See Fig. 17B, Fig 18, and col. 30 ln. 7-9) When the context is switched to window 3 and rwcp3 is asserted, both the INS

and the OUTS of window 3 are accessible. When rwcp3 is asserted in conjunction with one of the rps*_in lines, the data of the INS of window 3 will be read.

While Joy describe an architecture for sharing bit cells, any given context only has the capability to select from one of the "two possibly addressed cells" (col. 30, ln 15-16) associated with that context. Joy has not taught "a first control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is not included in the first set of data storage devices." Therefore, it is respectfully submitted that independent claim 1 is not anticipated by Joy and should be withdrawn.

As claims 2-4 are dependent on claim 1, all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 2-4.

Claims 5 and 11 recite:

> selecting the first thread associated with the first context...
>
> fetching a first instruction of the first thread...
>
> decoding the instruction to determine a second context and source data register associated with a first operand;

The invention beneficially allows a first thread to access information from the state of a different thread. For example, when executing an instruction from a first context one or more of the operands can be associated with a second context, where the second context has been determined by decoding the instruction.

In contrast, Joy teaches a system for rapidly switching between contexts. In the system taught by Joy, an instruction of a first context cannot use either source or destination registers outside of that first context. The context for data reads (and therefore operands) is determined by the current window pointer. As shown above, the current window pointer indicates the current context, that is, the context of the currently executing instruction. (See Fig. 16 and col. 28, ln. 55) Therefore, Joy does not disclose decoding the instruction to determine a *second* context.

For at least these reasons, it is respectfully submitted that the claimed invention is not anticipated by Joy and should be withdrawn.

As claims 6-10 are dependent on claim 5, all arguments advanced above with respect to claim 5 are hereby incorporated so as to apply to claims 6-10.

Accordingly, for at least the reasons set forth above, claims 1-11 are patentable over the cited reference. Thus, Applicants kindly request withdrawal of these rejections.

Conclusion

Applicants respectfully submit that claims 1 through 11, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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Date: Feb 6, 2008 By: _____

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